a third transistor of the secondary conductive type connected in series to the third transistor of the primary conductive type and operating based on a second signal from the second differential amplifier circuit,

wherein at least one of the first differential pair and the second differential pair is formed from a pair of transistors having a driving ability difference therebetween,

wherein the first differential amplifier circuit outputs the first signal in order to output a first output voltage lower than the common input voltage through the third transistor of the primary conductive type,

and wherein the second differential amplifier circuit outputs the second signal in order to output a second output voltage higher than the common input voltage through the third transistor of the secondary conductive type.

REMARKS

Claims 1-9 are pending in this application. By this Amendment, claim 1 is amended to correct a typographical error.

Entry of the amendments is proper under 37 CFR §1.116 since the amendment: (a) places the application in condition for allowance for the reasons discussed herein; (b) does not raise any new issue requiring further search and/or consideration; (c) does not present any additional claims without canceling a corresponding number of finally rejected claims; and (d) place the application in better form for appeal, should an appeal be necessary. The amendment is necessary and was not earlier presented because it is made to correct a typographical error. Entry of the amendment is thus respectfully requested.

The Office Action rejects claims 1 and 7-9 under 35 U.S.C. §102(b) as being anticipated by Andrews (Class AB Unity Grain Buffer Amplifier for CMOS Technology); and claims 1-9 under 35 U.S.C. §103(a) as being obvious over Saller (U.S. Patent No. 4,757,275) in view of Shulman (U.S. Patent No. 6,064,258).

In particular, neither Andrews, Saller nor Shulman, individually or in combination, disclose or suggest a differential amplifier including a first differential amplifier circuit having a first differential pair and operating based on a common input voltage, a second differential amplifier circuit having a second differential pair and operating based on the common input voltage at least one of the first differential pair and the second differential pair is formed from a pair of transistors having a driving ability difference therebetween, and wherein the first differential amplifier circuit outputs the first signal in order to output a first output voltage lower than the common input voltage through a third transistor of a primary conductive type, and the second differential amplifier circuit outputs a second signal in order to output a second output voltage higher than the common input signal through a third transistor of a secondary conductive type, as recited in independent claim 1.

The Office Action alleges that Andrews discloses in col. 1, third paragraph, a pair of transistors having a driving ability difference therebetween. Applicant has carefully reviewed the cited passage. However, nowhere in col. 1, third paragraph, does it disclose or suggest this feature of the claim. Instead, col. 1, third paragraph, merely states in general that in the amplifier circuit of Fig. 1, transistor sizes and bias currents are entirely arbitrary and will need to be adapted to optimize performance for a given application or a given process technology. However, this general statement is vague and fails to disclose or suggest at least one of the first differential pair and the second differential pair is formed from a pair of transistors having a driving ability difference therebetween, recited in independent claim 1.

Furthermore, the Office Action alleges that Fig. 2 of Andrews discloses the first differential amplifier circuit outputs the first signal in order to output a first output voltage lower than the common input voltage through the third transistor of the primary conductive type by using Vout at time from 0 to 0.5 mS of Fig. 2 as the disclosure; and the second differential amplifier circuit outputs the second signal in order to output a second output

voltage higher than the common input voltage through the third transistor of the secondary conductive type by using Vout at time from 0.5 mS to 1 mS of Fig. 2 as the disclosure.

On the contrary, Fig. 2 of Andrews merely discloses the input/output signal performance of the amplifier circuit of Fig. 1, but there is no teaching or suggestion that the performance graph is in anyway related to the first differential amplifier circuit outputs the first signal in order to output a first output voltage lower than the common input voltage through the third transistor of the primary conductive type, and the second differential amplifier circuit outputs the second signal in order to output a second output voltage higher than the common input voltage through the third transistor of the secondary conductive type, as recited in independent claim 1.

Saller discloses that to overcome a performance limitation in the buffer circuit shown in Fig. 2, one could create a symmetric version of the buffer circuit by duplicating the circuit using PNP transistors and tying their common points together, as shown in Fig. 3. The current source 13 in Fig. 2 is no longer needed since the buffer circuit has a symmetric output stage resembling a class AB push pull amplifier. This eliminates the dynamic performance degradation due to the unsymmetric and limited output drive capability of Fig. 2. This typology also improves the DC accuracy of the buffer. The offset voltage that is due to the Early effect between transistors 15 and 16 is reduced by the mismatch in base-emitter voltage of transistor 17 and 18 due to the Early effects. If the transistors 15, 16, 17 and 18 all have the same Early voltage, the offset is reduced to zero. Also, the bias current at the input is now equal to the base current of transistor 15 minus the base current of transistor 17. For equal values of current gain in transistors 15 and 17, and equal bias currents of current sources 19 and 20, the input bias current is also equal to zero. See, for example, Figs. 2 and 3 and col. 3, lines 42-64.

On the contrary, nowhere in Saller does it disclose or suggest the first differential amplifier circuit outputs the first signal in order to output a first output voltage lower than the common input voltage through the third transistor of the primary conductive type, and the second differential amplifier circuit outputs the second signal in order to output a second output voltage higher than the common input voltage through the third transistor of the secondary conductive type, as recited in the claim.

Further, the Office Action alleges that because Shulman discloses differential pair to be different for the purpose of having offset for an amplifier, Shulman discloses at least one of the first differential pair and the second differential pair is formed from a pair of transistors having a driving ability difference therebetween. Further, this feature would be inherent in Saller.

On the contrary, Shulman merely discloses that in Fig. 3, auxiliary amplifiers 303-1 and 305-1 each have the smallest design offset voltage, while auxiliary amplifiers 303-N and 305-N have the largest design offset voltage. The intermediate ones of the auxiliary amplifiers 303 and 305 have offset voltages that are determined by the circuit implementers.

Furthermore, Applicant refers the Examiner to MPEP §2112 where it is clearly stated that to establish inherency, the extrinsic evidence "must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it will be so recognized by persons of ordinary skill. Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may resolve from a given set of circumstances is not sufficient."

As discussed above, Shulman fails to disclose or suggest at least one of the first differential pair and the second differential pair is formed from a pair of transistors having a driving ability difference therebetween. Furthermore, what is disclosed in Shulman cannot be

inherent in Saller because inherency may not be established by probabilities or possibilities and must be necessarily present and the thing described in Saller.

For at least the reasons stated above, Applicant respectfully submits that independent claim 1 defines patentable subject matter. Claims 2-9 depend from independent claim 1, and therefore also define patentable subject matter. Accordingly, favorable reconsideration and prompt allowance of claims 1-9 are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in better condition for allowance, the Examiner is invited to contact Applicant's undersigned representative at the telephone number set forth below.

Respectfully submitted,

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APPENDIX

Changes to Claims:

The following is a marked-up version of the amended claim:

1. (Twice Amended) A differential amplifier comprising:

a first differential amplifier circuit having a first differential pair and operating based on a common input voltage;

a second differential amplifier circuit having a second differential pair and operating based on the common input voltage;

a third transistor of the primary conductive type which operates based on a first signal from the first differential amplifier; and

a third transistor of the secondary conductive type connected in series to the third transistor of the primary conductive type and operating based on a second signal from the second differential amplifier circuit,

wherein at least one of the first differential pair and the second differential pair is formed from a pair of transistors having a driving ability difference therebetween,

wherein the first differential amplifier circuit outputs the first signal in order to output a first output voltage lower than the common input voltage through the third transistor of the primary conductive type,

and wherein the second differential amplifier circuit outputs the second signal in order to output a ~~first~~ second output voltage higher than the common input voltage through the third transistor of the secondary conductive type.